17320

13141

3 Hours / 100 Marks Seat No. | | | | | | | | |

Instructions – (1) All Questions are *Compulsory.*

(2) Answer each next main Question on a new page.

(3) Illustrate your answers with neat sketches wherever necessary.

(4) Figures to the right indicate full marks.

(5) Assume suitable data, if necessary.

(6) Mobile Phone, Pager and any other Electronic Communication devices are not permissible in Examination Hall.

Marks

1. a) **Attempt any <u>SIX</u> of the following:** **12**

i) List any two nonweighted code.

ii) Write the functions of following ICS :

1) 74151

2) 74155

iii) Define modulus of counter. How many flip flops are required for mod 5 counter.

iv) List the types of shift registers

v) List the types of ADCs and DACs

vi) Compare RAM and ROM (any two points)

vii) State De Morgan's theorems.

viii) Why NAND and NOR are called as universal gates?

Marks

b) **Attempt any TWO of the following:** **08**

i) Write down rules for binary addition and subtraction.

ii) Design half adder using K Map

iii) Design 16:1 MUX using 4:1 MUX only

2. Attempt any FOUR of the following: **16**

a) Subtract using 2's complement

i) $(1101)_2 - (1001)_2$

ii) $(1000)_2 - (1010)_2$

b) Realise Y=AB+AC using one OR gate and one AND gate only.

c) Convert the given expressions into standard form

i) $Y = A + BC + ABC$

ii) $Y = (A + B)\ (A + \overline{C})$

d) Draw clocked SR flip flop with preset and clear using gates. What is the drawback of SR flip flop.

e) Draw 3 bit asynchronous up counter with truth table and timing diagram.

f) Draw 4 bit weighted Resistor DAC and give expression for output voltage. What is the advantage of this type of DAC.

3. Attempt any FOUR of the following: **16**

a) Perform BCD addition

i) $(37)_{10} + (65)_{10}$

ii) $(45)_{10} + (24)_{10}$

b) Compare TTL and CMOS with respect to propagation delay, power dissipation, fanout and basic gate.

Marks

c) Write down the truth table for the given diagram. Refer Figure No.1.

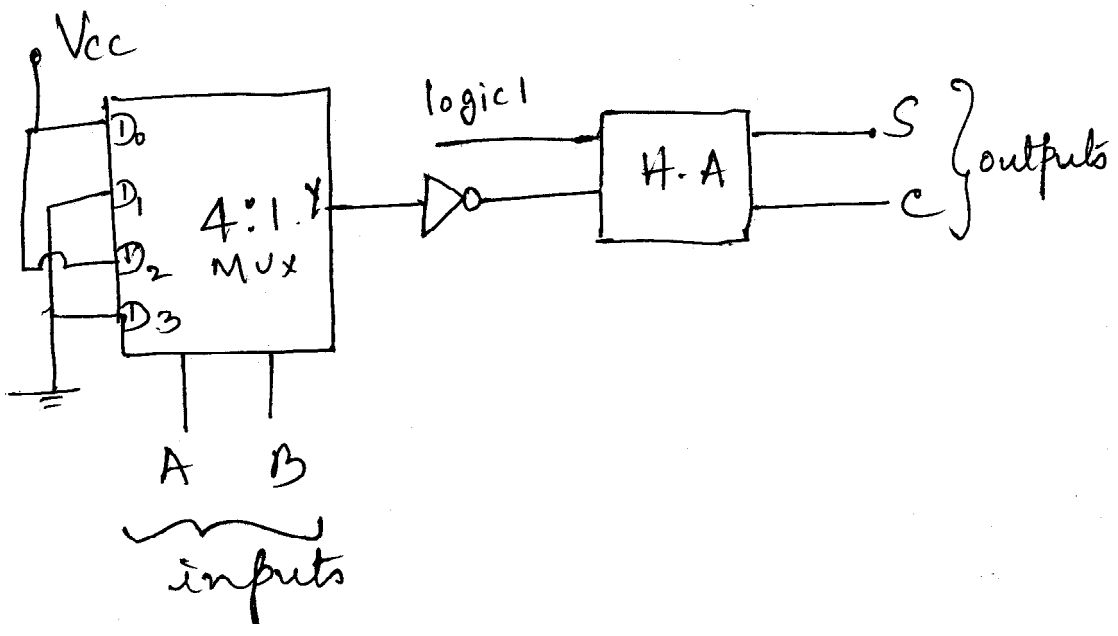

Fig. No. 1

d) Draw D and T flip flop using JK flip flop.

e) Describe the working of single slope ADC with block diagram.

f) Draw 4 × 4 memory organisation of ROM array and list the types of ROM

4. Attempt any FOUR of the following: **16**

a) Define tristate logic. Draw the symbol of tristate inverter.

b) Realise using 8:1 MUX f = $\sum(0, 3, 4, 7)$

c) What is race around condition in JK flip flop? How it is avoided using MSJK flip flop.

d) Draw 3 bit twisted ring counter using D flip flop. Give its timing diagram.

e) Draw and explain dual slope ADC

f) Compare static RAM and dynamic RAM, volatile and non volatile.

Marks

5. Attempt any <u>FOUR</u> of the following: **16**

a) Draw and explain TTL NAND gate with totempole output

b) Define priority encoder. Draw the truth table of decimal to BCD encoder

c) Write down excitation table for SR flip flop and T flip flop.

d) Design mode 6 counter using IC 7490

e) Draw and explain SAR ADC with block diagram.

f) Give classification of memory compare EPROM and Flash memory (3 points)

6. Attempt any <u>FOUR</u> of the following: **16**

a) Convert the given number into octal, binary, hexadecimal and BCD $(64.75)_{10}$

b) Two square waves of 2KHZ and 4KHZ are applied as the inputs of AND and OR gates. Draw the output waveform in each case.

c) Prove :

i) $A + \overline{A}B = A + B$

ii) $(A + B)(A + \overline{B}) = A$ using Boolean theorems.

d) Design 1:32 demux using 1:8 demux

e) Draw 3 bit synchronous counter with truth table and timing diagram

f) Derive the expression for output voltage in 3 bit R-2R ladder DAC

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